ECSE 222 – DIGITAL LOGIC

VHDL ASSIGNMENT 2

LAB REPORT

Group:

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# SUMMARY

In this assignment, we learnt to create a schematic gate diagram of a logic circuit using CAD tools on Quartus Prime, as well as write VHDL testbench based on the template file. We then synthesize the logic circuit/function and perform the simulation on ModelSim. (must paraphrase bc of plagiarism)

# QUESTIONS

1. Explain your VHDL code.
2. Report the number of pins and logic modules used to fit your designs on the FPGA board. These results can be obtained from the flow summary tab in the table of contents menu in Quartus.

|  |  |  |  |
| --- | --- | --- | --- |
|  | AeqB | 2-to-1 MUX | |
|  | Schematic | Structural | Behavioral |
| Logic Utilization (in ALMs) |  |  |  |
| Total pins |  |  |  |

1. Show a representative simulation plot for the introductory testing example. You can simply include a snapshot from the waveform that you obtained from ModelSim. In order to fully capture all the signals from the waveform, you can adjust the display range using the magnifier icons.
2. Show representative simulation plots for the exhaustive test.
3. Show representative simulation plots of the 2-to-1 MUX circuits for all the possible input values.

# FIGURES

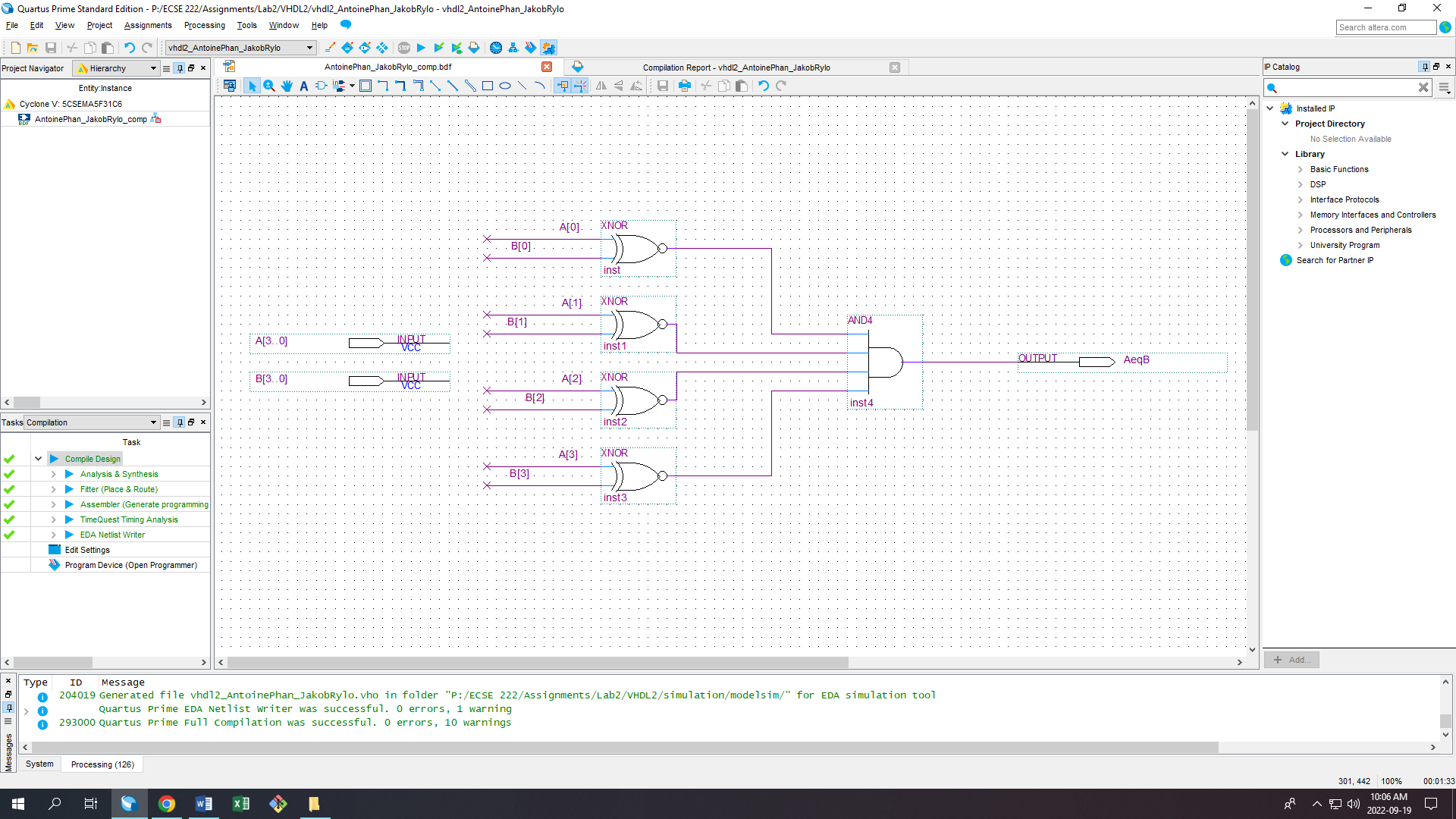


Figure 1: Schematic diagram design of the circuit

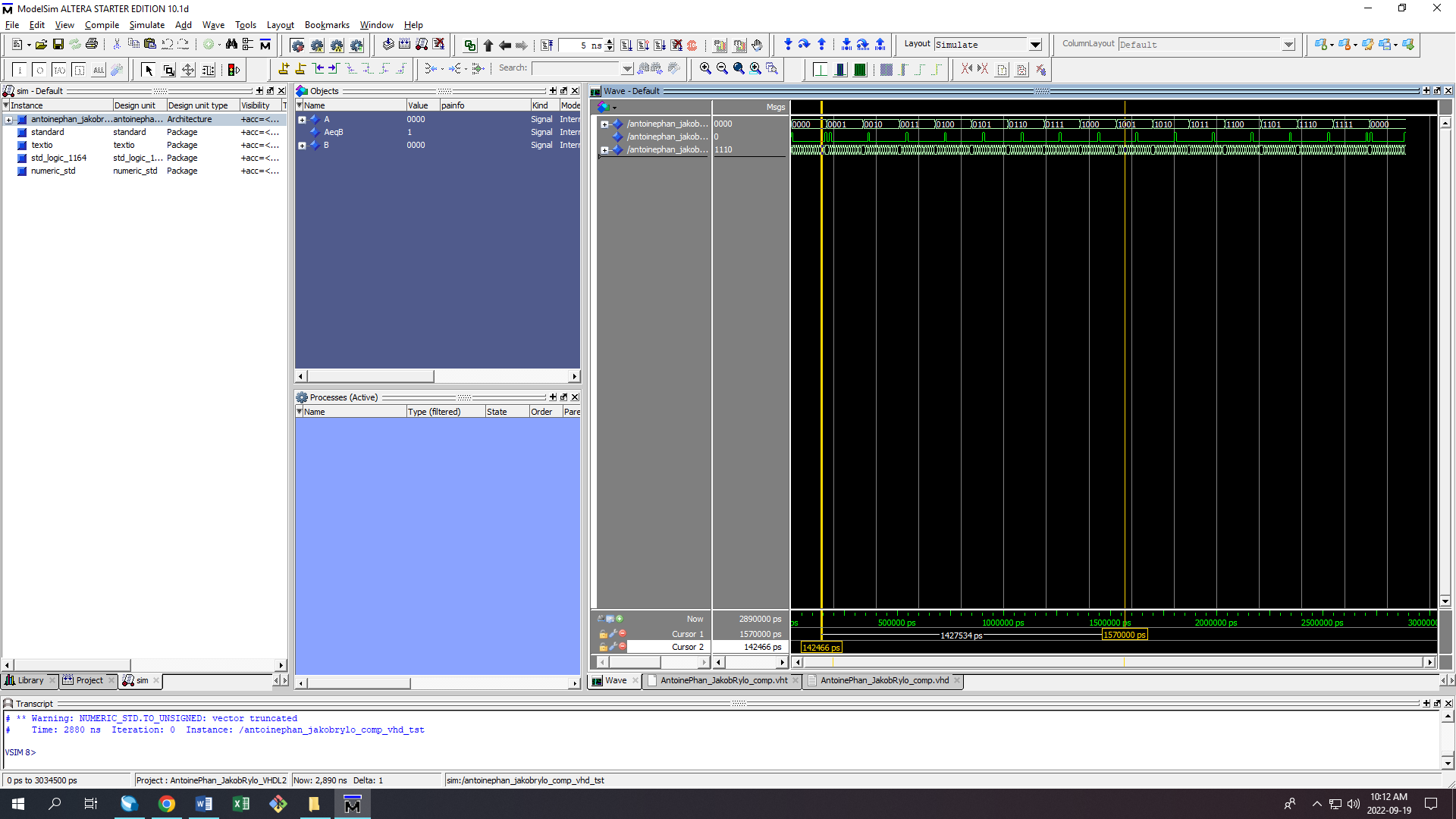


Figure 2.1: Simulation of the schematic diagram design on ModelSim (exhaustive test/brute force)

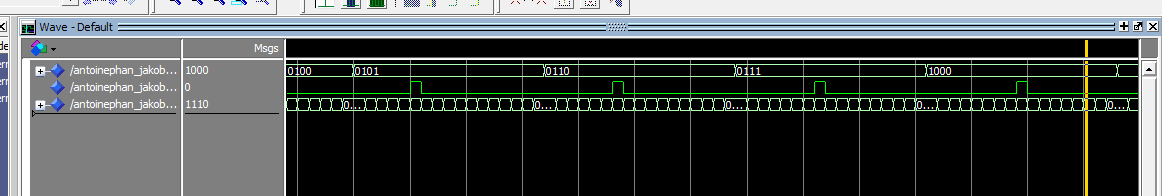


Figure 2.2: A close-up zoom-in of the simulation on ModelSim

# EXPLANATION

# CONCLUSION